Grenze International Journal of Computer Theory and Engineering , Special issue

Various Concepts Of Routing and the Evaluation Tools for NOC

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***Abstract*— This paper presents about the Network on Chip (NoC) and various concepts of routing and the evaluation tools used for it. As we know that the IC technology is scaling down day by day, Specifically the system on chip (SoC) i.e. the components present on the chip are scaled drastically every year therefore there is an increase in the complexity of the system this is due to the current requirements such as a device must be portable that means we have to optimize the area, low power consumption i.e. power optimization and also getting accurate results. To achieve these entire things one must go for in depth fabrication process by using the various technologies scaling hence there is an increase in the complexity. To avoid the routing complexities in such complex SoC devices we will go for NoC.**

***Index Terms*— SoC, NoC, MPSoc, Router, Network Adapter.**

I. INTRODUCTION

The transistors integration capacity are increasing per chip day by day ,as a result we entered into deep sub micron technology were the number of components are scaled in few nano's .The Figure 1.shows there is an increase in the growth of the transistors over a years on a single silicon chip.

System on Chip (SoC) designs will help to resolve the problems in space and technology, multimedia, consumer electronics etc. Due to the emergence of SoC technology tremendously, we are seeing the growth occurred in the technologies are great. Initially the SoC was consisting of a very few processing elements like DSP, FPGA, CPU, DAC, ADC, Processors, IP's etc. But nowadays SoC consists of multi processors SoC [MPSoC] to facilitate many functions at a time and the examples for such a system are laptop, PDA, mobiles, digital camera etc. If there is an increased in the number of elements then there will be an increase in the On Chip Communication which will leads to the complication in routing. Therefore we will switch to the NoC paradigms which will helps to solve the design engineer's problem in intra chip communication.

Creating an efficient on chip inter connect for MPSoC is difficult job for an engineer because which will leads to many complexities like synchronization with a single clock source, negligible skew, CPU's average latency & bandwidth etc[1-2].

In SoC initially the On Chip Communication was used to done with the help of buses, Which was nothing but the usage of wires for routing, these wires were going to create many problems in the back end design like :increase in the hardware due to the use of long global wires, it was difficult to manage the time, and

Grenze ID: 01.GIJCTE.3.4.64
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degradation of electrical performance due to the addition in the parasitic capacitance, limitation in the bandwidth and the bus latency etc. Therefore new routing methods are being adopted i.e. NoC which is being used widely today.
It separates communication from computation, it allows multiple voltages and frequency domains, and also it allows arbitrary number of terminals, which will help to optimize the power and area. It follows larger protocols and also helps in Customization. Which will includes size of the packet and topology being used [3- 6], [12].

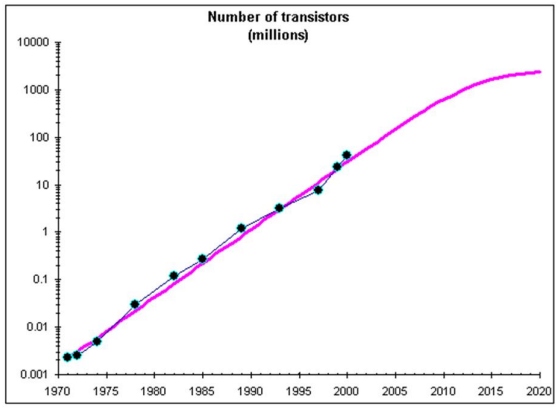


Figure 1. Increase in the number of transistors over a years on single silicon chip

II. NETWORK ON CHIP

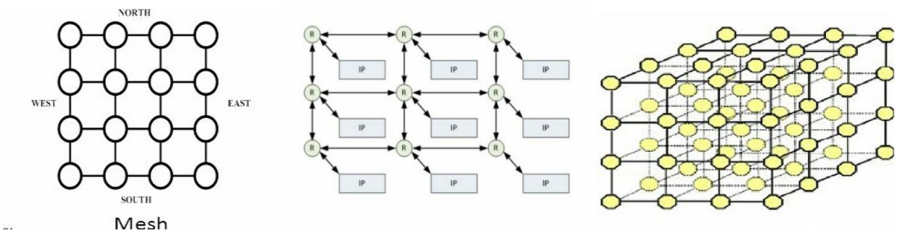
To overcome the problems in MPSoC we will go for NoC which is widely used in today's world. NoC will helps to give a guaranteed performance i.e. a maximum latency or a minimum bandwidth. It supports synchronization for both local variables and global variables, because of this it is able to provide a glitch circuit and also manages the clock arrival time.

A. Parts of NoC

The NoC mainly consists of three parts namely Router, Network Adapter/Network Interface and connectors.
Router: It helps to direct the packet which has to be sent based on the selected routing path.
Network Adapter: It helps to connect the two elements i.e. the data packet which mainly consists the information for processing the data and the router.
Connectors: These are used to transmit the data between the various elements on a system [4].

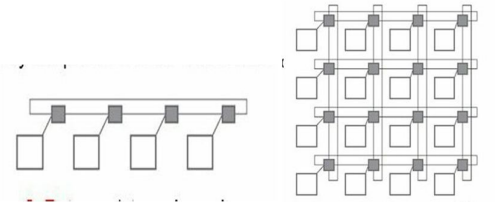
B. Topology

Topology is a way to define which components or units are physically connected to each other i.e. it is the schematic representation of a network. To achieve an effective communication there are various topologies are available in NoC architecture. There are mainly two types of topologies exists i.e. regular and irregular topologies. The below Figures from 2.1 to 2.4 show some regular topologies. The irregular topologies are also called as hybrid topologies. Which are the combinations of 2 or 3 regular network topologies.
Mesh topology: This is a regular network topology here every node will send the data to the network. The advantage of this is failure of a single node will not affect the whole transmission of data in a network, and it can also handle the high data rate. The disadvantage of this is difficult to handle it, since continuous observation is needed to check the errors .But the experts will solve these problems very easily. Some of the mesh network topologies are shown in Figure 2.1 like a) mesh, b) 2D-mesh & c) 3D-mesh.
Mesh torus topology: This is a regular network topology which is an improved version of mesh network topology. This is used to connect the nodes in a parallel computer system. There are many types of torus networks are available they are 1D, 2D, 3D, 6D & ND tours networks. The advantages of torus network topologies are to achieve a high speed, lower latency, and lower energy consumption .The disadvantage of torus network will be complexity in wiring & cost. Some of the mesh torus network topologies are shown in Figure2.2 like a) 1D mesh torus b) 2D mesh torus.



a) Mesh b) 2D mesh c) 3D Mesh

Figure 2.1 Mesh network topologies



a) 1D Mesh torus b) 2D Mesh torus

Figure 2.2 Mesh torus network topologies

Ring topology: It is a regular network topology and the structure of this is a closed path which forms the ring, hence the name ring topology. Here every node connects to the next node which is placed next to it and also it will connect with two nodes at a time which are placed next to it at both the sides. Here the load variations for a node will not degrade the performance of a network and this is a big advantage. The disadvantage will be if one node stops working then the entire network gets affected. The ring topology is as shown in Figure 2.3

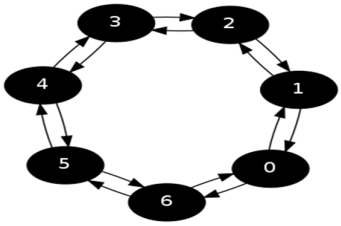


Figure 2.3: Ring network topology

Fat Tree: This is a kind of regular network topology. The structure of this will be in the form of tree which will be consisting of many nodes, it will create branches of same size. The communication speed will be increased if the root is kept closer to the nodes. If there are more branches on a tree are available then the communication path will be reduced this is an advantage of fat tree topology. And the disadvantage of this will be, it is going to be complex for external communication since there is a huge gap in between the root and the top node. The fat tree network topology is as shown in Figure 2.4.

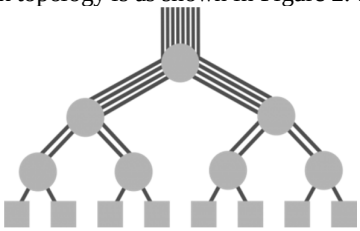


Figure 2.4 Fat Tree network topology

C. Routing

In routing transmission of data from source to destination has been achieved. To avoid the circuit switching disadvantages the new methodology has been introduced i.e. packet switching, here the data is sent in terms of packets. By using this we can achieve improvement in connectivity. It helps to increase the scalability of the interconnect network & most of the NoC's are based on the stable routing techniques like XY routing, this is one of the basic routing mechanism where the packet will move in the XY directions depending upon the need .It fails to transmit the data in case of breaks in the link.

There is one more kind of routing technique is available called Automatic Routing. As the name says it will helps to find the new ways automatically in case of path change .Further this automatic routing can be achieved in two different ways .first one is by keeping the information of neighboring nodes and its path. The second way will be done by knowing the entire network connection along with its specified path. Compare to first one the second way is more beneficial [4-5], [10].

D. Router Architecture

Generally routers consists of the several network interfaces to the attached networks, processing modules, buffering modules and an internal inter connection unit (or switch fabric). Routers can be implemented for various functions from simple switching to complex routing. There are two types of routing architectures are available mainly i) circuit switched network, ii) packet switched network.

Closed circuit network: It is a kind of network which is mainly used when the path is specified for a particular connection i.e. for the fixed paths. One simple example for this kind of network will be landline telephone connection that is at a time we can make only one call during that period the path will be fixed for Particular network.

Packet switched network: It is a kind of network here the information to be sent in the form of small units called packets. Here the whole information is sub divided into the number of sub units called packets and each packet consists of the address path .The advantage of this will be the same path can be used by the other users also and the best example for this will be the transmission control panel (TCP).Many NoC network architectures are based on packet switching type, which will gives a fair idea for designing of routers for NoC [5], [8].

E. Routing Protocols

Unicast Routing Protocol: Here the final destination is only based on the routing design. It follows the point to point communication. The unicast routing can be achieved in many ways based on the decision taken.

Concentrated Routing Protocol: In concentrated routing protocol the main processor of the system will be running based on the middle node or the major node. This major node will be having the information of all other nodes. By keeping this information the routing paths will be assigned to all other nodes. This can be achieved by making use of tables to gather the information accurately.

Origin Routing: In the Origin Routing we can see that it will be consisting of the entire routing links starting from the origin of a network to the end points of the network.

Distributed Routing Protocol: It is a kind of automatic routing protocol. Here each unit in a network system has the ability to make their own routing pathway. Based on the nodes cooperation they are further categorized into cooperative and non cooperative nodes. Cooperative nodes can share the links with other nodes. But non cooperative nodes will not share the links to the other nodes.

Multiphase Routing or *Hybrid Routing*: If more than one root are available at the origin node. Then the origin node will calculates the all possible paths based on the distance .Then it will choose the simplest possible path to send the information.

*Path Decision making algorithms:*These can also be implemented based on their hardware designing. Decision makings should be done fast in case of multiphase routing therefore there is a need of designing a perfect hardware. Most commonly used hardware designs are look up table and FSM.

- *Look up Table:* These are more popular type of path decision making algorithms. The looks up tables are being implemented in software, where every node consists of a Look up Table (LUT).
- *FSM*: It stands for finite state machine. It can be designed both in terms of hardware as well as software. Further which is used to run the applications based on the hardware as well as software. Here the path decision will not only including the addresses but also other factors.

Determined Routing: Here it is going to generate the same routing path for both source and destination. Where the path is going to be fixed or determined. By using this kind of routing we can achieve the high data transmission. Usually it is being used for small distances. The advantage of this will be, we can achieve the error free routing. This technique is mainly used in supercomputers. Exactly it will be used to provide the interlink connections in a supercomputer. These routing algorithms are costly to implement and also resulting in the increase of area cost therefore we must set right QoS metric before adopting these algorithms [5].
Back tracing algorithm: It is used to find the solutions to some computational problems. Like to find out the faults in a path, that is this can be used as fault-tolerant algorithms.
Misrouting algorithm: Here this will not see the distance it will sends the flits directly to the destination. Even though which is away from it. It will see the number of paths available for routing further these routing algorithms are classified into complete and partial.

F.Switching Techniques

Switching techniques tells about the how the routing has been done from origin node to the end user. These are mainly classified as closed circuit network and packet switched network.
In closed circuit network routers are designed with no queuing because there is fixed lines are available for communication. In packet switching we can send the data to multi paths at a time here the path is not reserved entirely, this can be further classified into wormhole switching, keep the information and send the data to the destination & Indirect transmission of data.
Keep the information and send the data to the destination: First the data is divided into several packets since it is a type of packet switching .here each packet will be consisting of its own path. Once the packet is reached to the particular node the path information will be stored in the buffer. This information will be used to send the packet to the destination. Mainly the information will be consists of source and destination address. If the path is error free then finally the packet will be sent to the destination.
Indirect Transmission of data: This one is also a type of packet switching. Here also first the data is divided into several packets but here the path information will be stored in the first byte of the packet and then the packet transmission will gets initiated as soon as it gets the path information the process begins. It won't check the entire packet it only see the path information if suppose there are some errors in the packet then it will be a disadvantage because at the end user is going to receive the corrupted data.
Wormhole switching: This technique does not direct any path or route to reach some specific destination over the network. However, it only makes a decision about the timing for routing packets from the router [3-5].

G. Quality of Service

It refers to the maximum ability of the network to give better service to a selected network, like achieving maximum bandwidth .In networks quality of service gives the idea about the speed of the transmitted bits .it includes both uplink and downlink transmission rates, and also it will includes latency and some other factors also to give better quality of services for a given network.

H. Circulation of Information

This is a technique of circulating the information, among the two nodes in a network. So that the data can be handled efficiently.
It will give the information about the channel size in terms of bandwidth, size of the buffer and the path information which is used to transmit the data through the network. This will be achieved in 2 ways i.e. with memory or without memory. In with memory the path information will be stored in the buffer but where as in without memory the path information will not be stored .this will be having more delay and less through put than compare to with memory [5].

III. NOC RESEARCH AREAS

The NoC research areas are classified as system level, network level & link level.
System level: Here the research is mainly concentrated at the architecture (network) level, the current NoC's are becoming more complex, and hence more difficulties will occur during test and evaluation process. The research areas for NoC's at the system level are design methodology and abstraction, architectures system comparisons, clustering & reconfigurability, traffic characterization, latency- critical, data stream ,through put, power consumption & space.

Network adapter (NA): it will come in the network core part and which will helps to makes communication services to be done. The research areas in network adapter are: the process of enclosing a device, designing of cavity etc.
Link level: it helps to link one processing element to the other processing element it will be having more than one channel. Research areas for link level are related to encoding, pipelining & synchronization issues.

A. Tools for NoC

The tools will vary based on the reason they built for. One can classify these tools as synthesizers and simulators further. In general we will do the simulation process first and later we will go for synthesis part.
*Synthesizers:*This will test the accuracy of the hardware part that is being generated .the accuracy of the hardware will be tested from top to down of the abstraction level .To achieve great speed of evaluation one must go for higher level of abstraction.
Simulator: It includes mainly two factors power design estimation & performance computing i.e. in terms of through put, latency & reliability. NoC simulator & it is building on top of Noxim Integrates Hotspot.
*NS:*It is an event simulator mainly used in the networking & it will helps to achieve the simulation of TCP, routing and multicast protocols over wired & wireless (local & satellite) networks. It is a type of real network simulator & it is introduced in the year 1989 and the new versions of NS are released into the market they are NS-2 which was first released in 2007 and it is written in C++.Now recently NS-3 is released into the market.
BookSim: It is a kind of network simulator .which is mainly used to test the accuracy of the network interlinks. It supports C++ language. It is mainly used to analyze the high end microprocessors.
WormSim: It was introduced in 2005, it is written in C++ &it supports 2D mesh and torus topologies.
Noxim: It is used to analyze the basic regular network topologies with the help of size of the network and routing algorithm. It was introduced in 2005.
NIRGAM: It was proposed by the University of Southampton in 2007, it is written in System C, and it supports 2D mesh, torus topologies and it also supports XY routing.
DARSIM: It is developed by an American university and this tool allows the torus network to simulate.
Access Noxim: This tool is developed by national Taiwan University in 2013, it supports C++ language and it is 3D
GEM5: It is proposed by an American university and some industries, which is written in C++, it is a NoC Multi Core simulator.
Orion: It is the power performance simulator for on-chip interconnection network. The successor of Orion is Orion 2.0 which is introduced in 2003 and it will helps to evaluate greatly [4], [13].

B. Evaluation Techniques for NoC

The evaluation process of NoC can be done by evaluating the factors like silicon area, power consumption and latency. If we will minimize all of these factors then we will get better results .Further if we want more accurate results then one has to understand how the optimization of the system can be done which is mainly used in the high end systems [6].
Some Specified NoC Proposals
Here we will see some specified NoC architectures which are found in the open literature.
Aethreal: The early work on AETHREAL was done in America .This will help to give real time requirements and also helps in achieving high performance at low cost. The best examples for this will be LED TV [3].
Spin Noc: This NoC is based on fat tree topology. And this is mainly used in supercomputers to achieve high level of communication
QNoC: It will help in providing different services for the user the QNoC will support regular network topology and it will supports for switching techniques also.

IV. CONCLUSION

The NoC separates communication from computation. And it will helps to solve the routing complexities in the high end processors like MPSoC's by adopting various network topologies and routing schemes which will further helps to increase the productivity. Researchers are well addressed about the router architectures and also tools for NoC by which evaluation of the NoC system can be done by using appropriate simulators and synthesizers. By using these things we will come to known the various complexities those will really matter and those can be minimized by optimizing various factors like area and power. And also by reducing

the latency etc. Network on Chip is one of the most active research area in many fields like embedded systems and networking.

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